SINGLE-PHASE CONTROL FOR CYCLOCONVERTER

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ABSTRACT

The output of a cycloconverter must exhibit proper amplitude, frequency, and wave form, simultaneously, for any particular condition of load operation. The cycloconverter produces the proper output waveshape by taking samples of power input voltage and assembling those samples in proper order. A voltage-controlled oscillator (VCO) generates a controlling voltage waveshape out of the cycloconverter. The frequency of this oscillator is linearly proportional to a control voltage at its input. The trigger signals for the SCR switches are formed by voltage comparison between the VCO output signal and a cosine-shaped sawtooth wave that is synchronous with the input power frequency. Power factor control circuitry modifies the SCR gate signals so as to allow proper SCR current flow into the load over varying power factor ranges.

INTRODUCTION

The output voltage of a cycloconverter must exhibit proper amplitude, frequency, and waveform, simultaneously, for any particular condition of load operation. These properties are maintained by control circuitry in response to an input analog control voltage. The method of generating the basic control waveform is such that either constant voltage or constant volt-second area of the waveform may be preserved at all frequencies within the control range. In applications where the cycloconverter drives lighting or heat-producing loads, constant voltage output may be desirable. The alternative constant volt-second output is desirable where a variable frequency is required for driving loads that operate by magnetic induction. The most important device in this category is the induction motor when used for speed drives. The cycloconverter produces the proper output waveshape by taking samples of the power-input voltage and assembling these samples in proper order. Since the output waveshape is composed of a series of samples, its spectral content contains both the desired frequency and also undesired components that are related to both the input power frequency and the desired frequency. These undesired components may be moved up in the spectrum, and thus further away from the desired component, by utilizing a larger number of samples. A polyphase input power source is more desirable than a single-phase source, since a greater number of samples is allowed in the output wave. The use of a polyphase source also allows the desired output frequency to more closely approach the power source frequency. In addition, the polyphase source allows a more favorable utilization of the current ratings of the power-switching devices in the cycloconverter.

The block diagram of the control for a cycloconverter is shown in Fig. 1. A voltage-controlled oscillator (VCO) generates a controlling voltage waveshape that determines the amplitude, frequency, and waveshape out of the cycloconverter. The frequency of this oscillator is linearly proportional to the control voltage, e_C, introduced as its input control terminals. An outstanding feature of the oscillator is that it generates the equivalent of a full wave-rectified sine wave, as shown in Fig. 2D, rather than a sine wave itself. The excursions of this wave are zero volt and an adjustable positive peak value, typically 3 volts. These limit values have a tolerance of a few millivolts. By generating a full wave rectified signal directly, all the half-cycle segments are identical. This expedient allows the DC component of the power switching banks in the cycloconverter to balance out to zero. In addition, it eliminates even-order harmonics in the output that result from the control signal. Both the DC and low frequency even-order components, if present, could produce an undesirable power loss in the load. In

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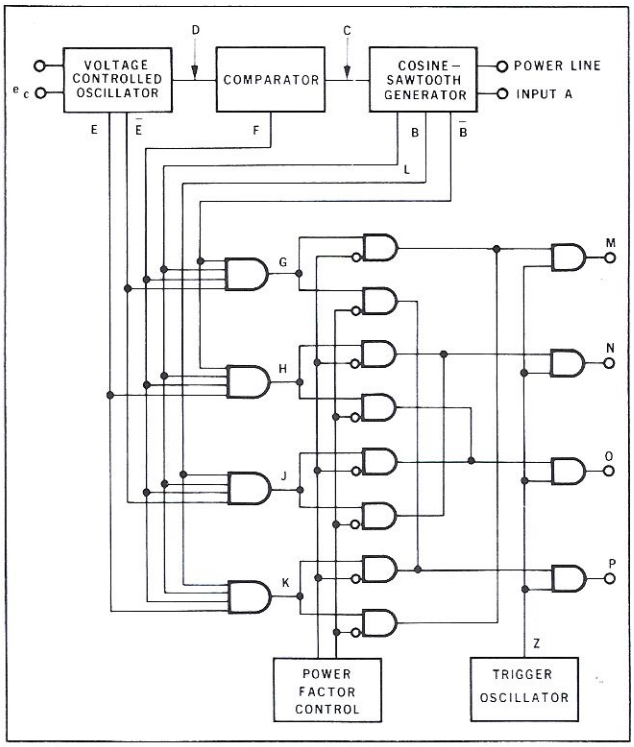

Fig. 1. Block diagram of control for cycloconverter.

addition to the rectified sine wave output, the VCO also furnishes a pair of complementary gating signals (one of which is shown in Fig. 2E). The phase relation between the rectified sine wave signal and the complementary gating signals is inherently maintained constant in the VCO (as shown in Fig. 2).

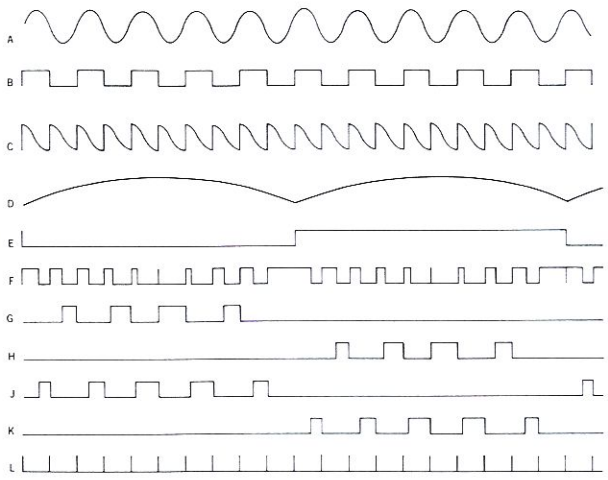

Fig. 2. Waveforms in control circuitry.

The trigger signals for the SCR switches, in the power handling portion of the cycloconverter, are formed by voltage level comparison between the VCO output signal and a cosine-shaped sawtooth wave that is synchronous with the input power frequency. The use of a cosinusoidal sawtooth rather than a linear sawtooth results in a more linear transfer characteristic of the control section, and thus less overall distortion of the desired power output signal from the cycloconverter. (The cosine-sawtooth wave is shaped in the cosine-sawtooth generator shown in Fig. 1.) The desired output from this generator is one that retains constant peak-to-peak amplitude with changes in the input power line voltage. For proper comparison with the VCO signal, the negative peak of the wave must be accurately clamped to the zero volt-level. Level comparison between the VCO output signal and the cosine-sawtooth wave (shown in Figs. 2D and 2C, respectively) is performed by a differential comparator. Fig. 2F shows the output of the comparator.

In addition to the cosine-sawtooth output, three other output signals are obtained from the cosine-sawtooth generator. These outputs consist of a pair of complementary gating signals (one of which is shown in Fig. 2B) and a blanking signal (Fig. 2L) which is effective during the cosine-sawtooth blanking interval.

The comparator output signal contains the gate control signals for all the SCR switches. The distribution of the groups of control signals contained within this composite signal is accomplished by NAND gates and the appropriate gating voltages. The signals designated as E and $\overline{E}$ in Fig. 1 control the formation of the positive and negative half-cycles of the output signal, while signals B and $\overline{B}$ allow full wave operation from the power line.

The output signals from the control gates are directed to the proper SCR in the positive and negative groups through four, single-pole, double-throw switches that are formed from eight interconnected inhibit gates. These inhibit gates are activated so as to allow proper SCR current flow into the load over widely varying power factor ranges. A pair of complementary gating signals derived from the power factor control circuitry provides the inhibit signals for the gates. The resulting gated outputs are then used to modulate a CW carrier signal that finally gates the SCR's. The use of a gated carrier rather than the gate signal itself eases the problem of coupling through an isolation transformer into the SCR gate terminal. The signals M, N, O, and P in Fig. 1 at the output of the modulator gates are used to drive four amplifier stages that provide the required gate driving signals for the SCR's.

VOLTAGE-CONTROLLED OSCILLATOR

The schematic diagram of the voltage-controlled oscillator is shown in Fig. 3. The input control voltage, which determines the operating frequency, is introduced at the input terminals of a pair of cascaded unity gain operational inverters. These inverters are marked $-A_1$ and $-A_2$ and utilize μA702's. The voltage e_C may have any value from 0 to -3 volt. The output of $-A_1$ will follow the input, but in a positive direction from 0 to +3 volt. A pair of single-pole,

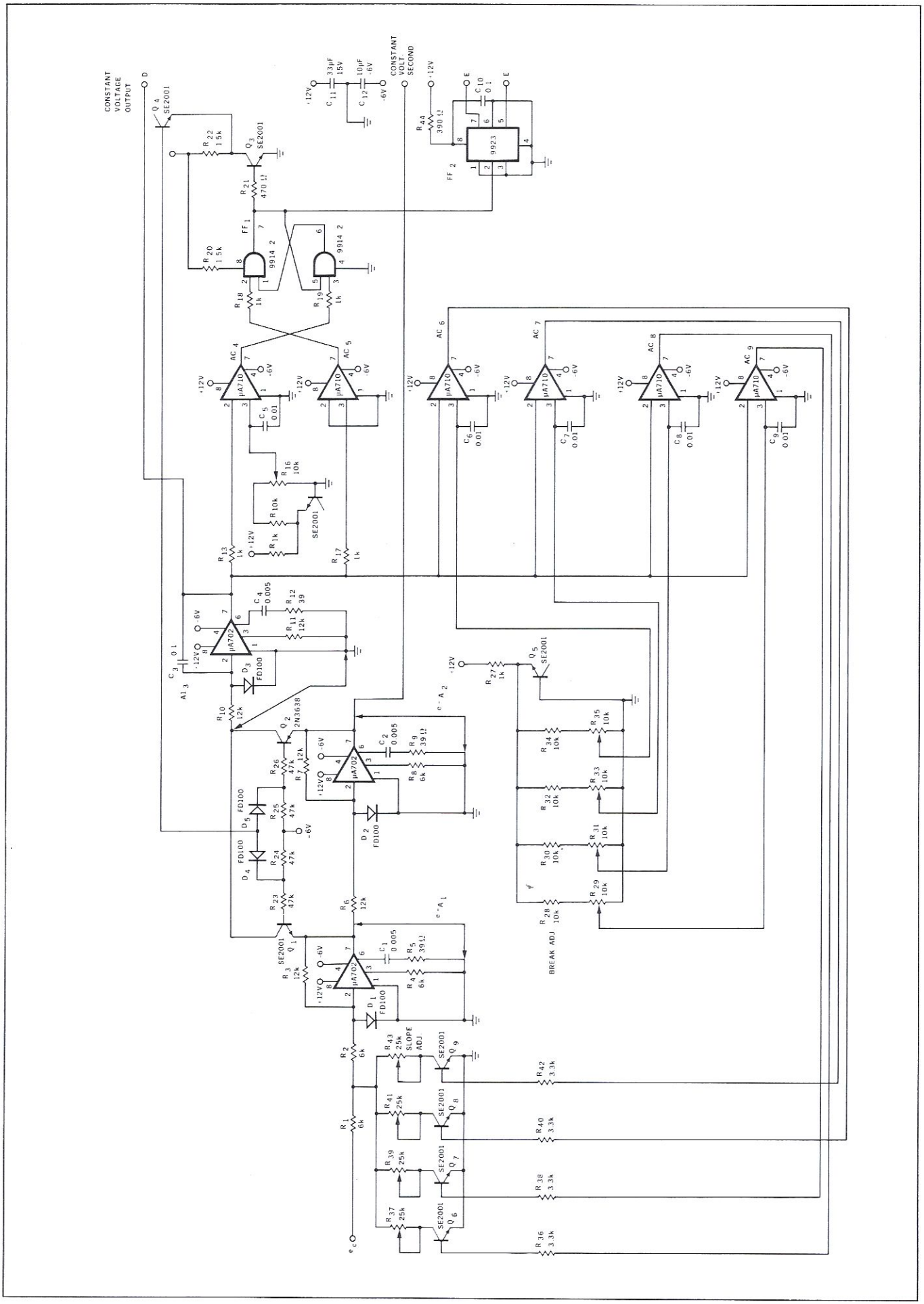

Fig. 3. Schematic diagram of voltage-controlled oscillator.

single-throw switches composed of transistors Q_1 and Q_2 alternately connect the output of $-A_1$ and $-A_2$ to the input of an operational integrator, AI_3, utilizing a μA702. Depending upon whether switch transistor Q_1 or Q_2 is conductive, the output of the integrator will display either a positive or a negative slope (as shown in Fig. 4). The peak positive and

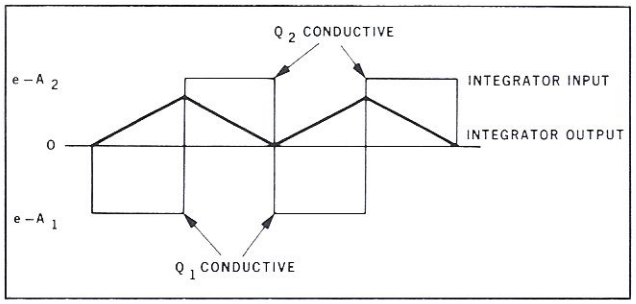

Fig. 4. Waveforms in basic integrator.

negative excursions of the integrator output signal are sensed by a pair of voltage comparators, AC_4 and AC_5, utilizing μA710's. The triangular voltage input to the positive limit comparator is introduced at the noninverting input with an adjustable positive voltage supplied to the inverting terminal. Thus, when the triangular voltage slightly exceeds the positive reference voltage, the output of AC_4 swings in a positive direction. Similarly, the negative excursion is sensed, but in this case, the triangular voltage is supplied to the inverting input terminal of the μA710 and the low limit reference voltage of zero volt is connected to the noninverting terminal, resulting in a positive output excursion for zero voltage limit sensing. Both of these positive-going signals are used to provide the set and reset for the toggle flip-flop (FF_1 in Fig. 3). The output of this flip-flop is buffered by a single-stage inverter utilizing transistor Q_3. The large voltage swing required for actuating the switch transistors, Q_1 and Q_2, is provided by this stage, while the required DC offset is provided by the zener diode consisting of the reverse-biased base-emitter diode of transistor Q_4.

The above described portion of the voltage-controlled oscillator results in a regenerative feedback loop that sustains oscillations in response to an input control voltage. The slopes of the triangular-voltage wave at the integrator output are directly proportional to the input control voltage, while the peak values of the sawtooth voltage remain constant as set by the limit voltages. Thus, the period is inversely proportional to input voltage, resulting in a direct proportionality between input voltage and frequency.

The trangular wave is modified to a rectified sinusoidal shape by changing the original slope at selected points along the wave. This is accomplished by first selecting the amplitude level (break point) at which the slope change should occur and then reducing the current into the integrator at the selected time. If this procedure is repeated a sufficient number of times, a close approximation to a sinusoidal shape results. The breakpoints for the slope change are determined by a group of voltage level comparators utilizing μA710's AC_6, AC_7, AC_8, and AC_9 (Fig. 3). The break-point voltages are adjusted by potentiometers R_{29}, R_{31}, R_{33}, and R_{35}. The voltage supplied to these adjustments is regulated by the zener voltage drop across the reverse V_{BE} (voltage base-to-emitter) of transistor Q_5. Since the triangular wave is introduced on the noninverting terminals of the comparators, the comparator output voltages swing positive when the break-point voltages are exceeded. This should occur in a successive manner. The output voltage from any single comparator remains positive as long as the triangular wave exceeds the break-point level. On the negative slope of the triangular wave, as its level becomes slightly more negative than the break-point level, the comparator output voltage swings to a low negative level from the previously attained positive level. Thus, the comparator output voltages contain break-point level information that is effective on both the positive and the negative slope of the triangular wave. These voltages are then used to switch in current shunting resistors at the input to the first operational inverter, $-A_1$. The switches consist of saturating transistors Q_6, Q_7, Q_8, and Q_9 connecting the adjustable current shunting resistors R_{37}, R_{39}, R_{41}, and R_{43}, respectively. As these current shunts are successively actuated, the output voltages of both inverters, $-A_1$ and $-A_2$, (as shown in Fig. 5) are designated e_{-A_1} and e_{-A_2}, respectively. Also shown are the integrator input, e_x, and output, D, signals, when the current shunting at the input is effective.

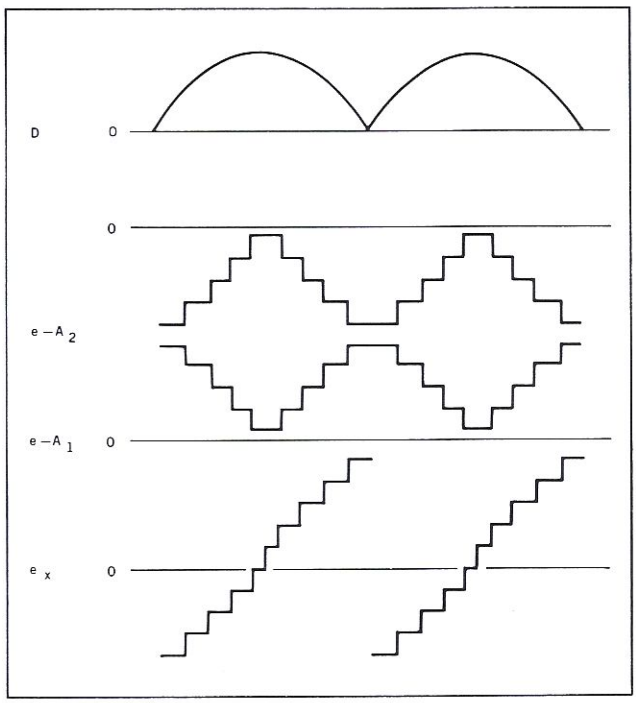

Fig. 5. Waveforms in integrator inverter.

The complementary gate output signals, E and $\overline{E}$, are obtained from the binary divider FF_2 utilizing a 9923 J-K flip-flop. The trigger signal for this stage is obtained from FF_1, the memory toggle for the integrator input switches. The phase relation between these complementary gating signals and the rectified sinusoidal output signal (shown by the waveforms in Fig. 2). If it is desired to use a constant volt-second output rather than the constant voltage output, the phase of the gating signals must be shifted 90 degrees. This may be accomplished by taking the input for the FF_2 from pin 6 on FF_1 rather than from pin 7.

COSINE-SAWTOOTH GENERATOR

The schematic diagram of the cosine-sawtooth generator is shown in Fig. 6. This portion of the overall control circuitry utilizes a larger percentage of discrete rather than integrated components because of the many simple functions required. The driving signal for the generator is derived from a step down transformer, T_1, operating directly from the power input line. By use of a center tapped secondary, a push-pull signal is obtained which is used to drive two separate portions of the generator: the cosine-sawtooth generating circuitry and the line synchronous complementary gating signal circuitry.

The push-pull voltage is full wave rectified in diodes D_1 and D_2 to provide a driving signal synchronous with each half-cycle. This rectified voltage is then clipped by the peak limiter, consisting of resistor R_1 and diode D_3, and applied to a voltage comparator consisting of transistors Q_1 and Q_2. As the comparator is referenced to ground potential, only the extreme negative peaks of the full wave rectified signal result in an output voltage at the collector of Q_1. This positive-going pulse is used to turn on switch transistor Q_3, which discharges the sawtooth-forming capacitor, C_1. The charge current source for C_1 is implemented by transistor Q_4. A constant value of charge current is maintained by the zener characteristic of the reverse base-emitter diode of transistor Q_5. In addition to the DC current through transistor Q_4, a rectified sinusoidal component is produced by coupling an appropriate current source into the emitter of Q_4. This current component is provided by resistors R_{12} and R_{13} and the rectified voltage source at the junction of diodes D_1 and D_2, while capacitor C_2 provides only AC coupling. The sinusoidal component of current into the capacitor results in a cosinusoidal voltage component across the capacitor C_1 as a result of the integration process. The resulting cosine-sawtooth across capacitor C_1 may be adjusted for peak amplitude by variable resistor R_{11}, which controls the DC charging current, while the amplitude of the cosine component is controlled by variable resistor R_{13}.

This method of forming the cosine-sawtooth allows the use of simple circuitry and ease of adjustment. However, before the voltage wave-shape can be utilized in the gate signal generating comparator, it must be inverted and its negative peak clamped very close to the zero voltage level

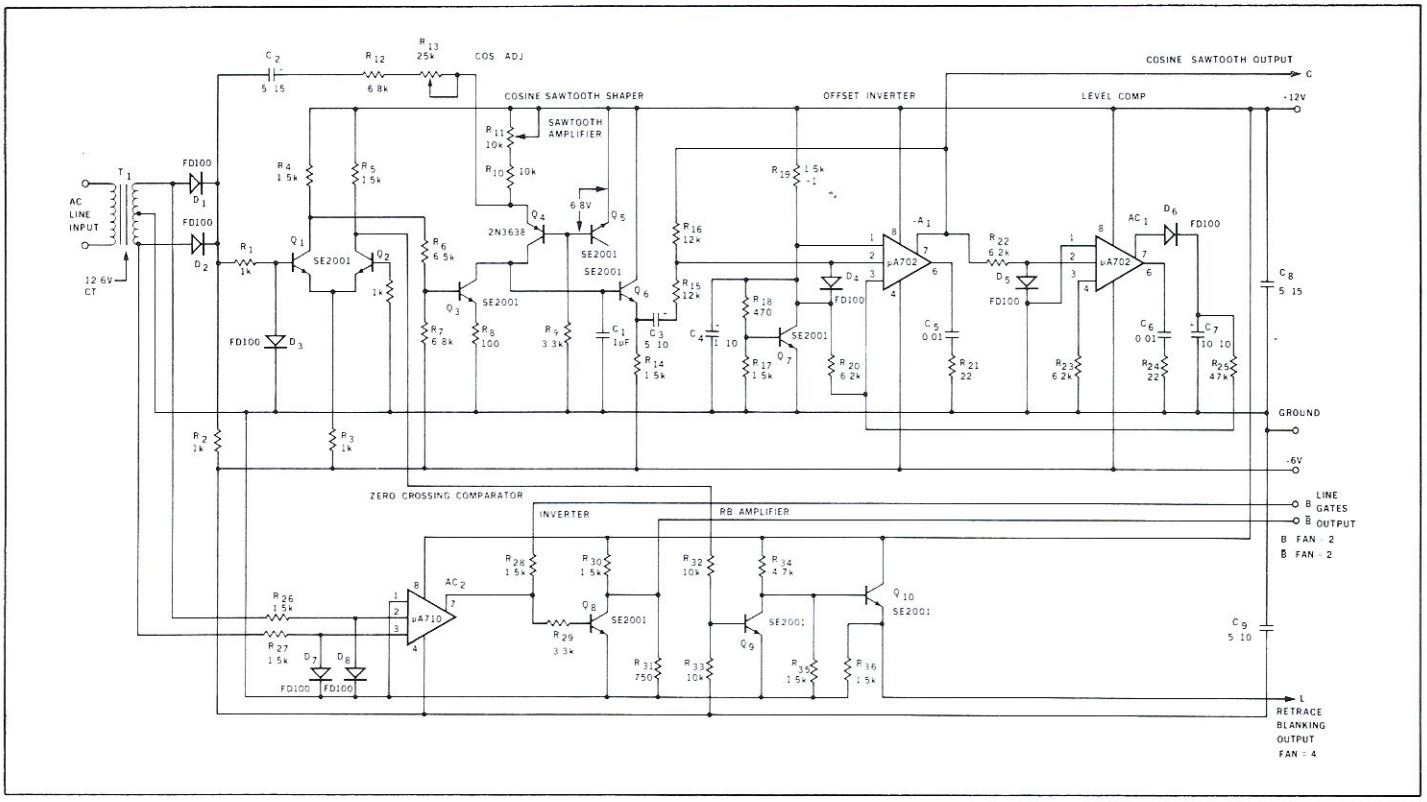

Fig. 6. Schematic diagram of cosine-sawtooth generator.

(as shown in Fig. 2C). The polarity inversion is accomplished by a unity gain inverter stage utilizing a μA702. This stage also provides a DC offset to the negative slope cosine-sawtooth wave at its output by means of a DC feedback signal applied to its noninverting input on pin 3. The ground terminal, pin 1, of the μA702 must be elevated +1 volt above ground potential to accommodate the positive DC component on pin 2 and the positive DC feedback voltage on pin 3. Transistor Q_7 provides the required regulated +1 volt source at pin 1 of the μA702. The DC feedback voltage that provides the proper offset to the cosine-sawtooth voltage waveshape at the output, pin 7, of the offset inverter is generated in a level comparator stage, AC_1. By comparing the negative-going edge of the inverted cosine-sawtooth voltage to a ground potential reference, an error voltage is developed that is proportional to the difference voltage. This signal consists of a train of positive-going pulses at the output, pin 7, of the level comparator. The peak voltage level information of this pulse train is recovered as the DC feedback signal by peak rectification in diode D_6 and capacitor C_7. This voltage is then applied to pin 3 of the offset-inverter through resistor R_{25}. The voltage appearing at the output, pin 7 ($-A_1$) of the offset inverter is the negative slope cosine-sawtooth voltage whose negative peaks are maintained at the zero voltage level and, as such, may be applied to the gate generating comparator.

The second portion of the cosine-sawtooth generator generates the line synchronous complementary gating signals for use in the distribution of the SCR gating signals. These complementary gating signals are generated by comparing the input line signal to its own zero crossing level. The push-pull line signals are applied to pins 2 and 3 of a μA710 (AC_2) comprosing the zero crossing comparator. The resulting output at pin 7 of the comparator is a symmetrical square wave that provides the line complementary gating signals, B in Fig. 2. The complement of this signal (B) is formed in an inverter stage utilizing transistor Q_8.

An additional signal is also provided in the cosine-saw-tooth generator for blanking the SCR gating signals during the retrace interval of the cosine-sawtooth voltage. This expedient prevents a short circuit condition through a pair of SCR's across the power line due to an undesired gating action during the retrace interval. The retrace blanking signal, waveform L in Fig. 2, is derived from the collector of transistor Q_2 in the comparator.

Waveform L is then level-shifted and given an improved rise time in the inverting amplifier utilizing transistor Q_9. The signal is buffered by an emitter follower, transistor Q_{10}, to provide an adequate high fanout for driving all gates in the SCR gate distribution circuitry.

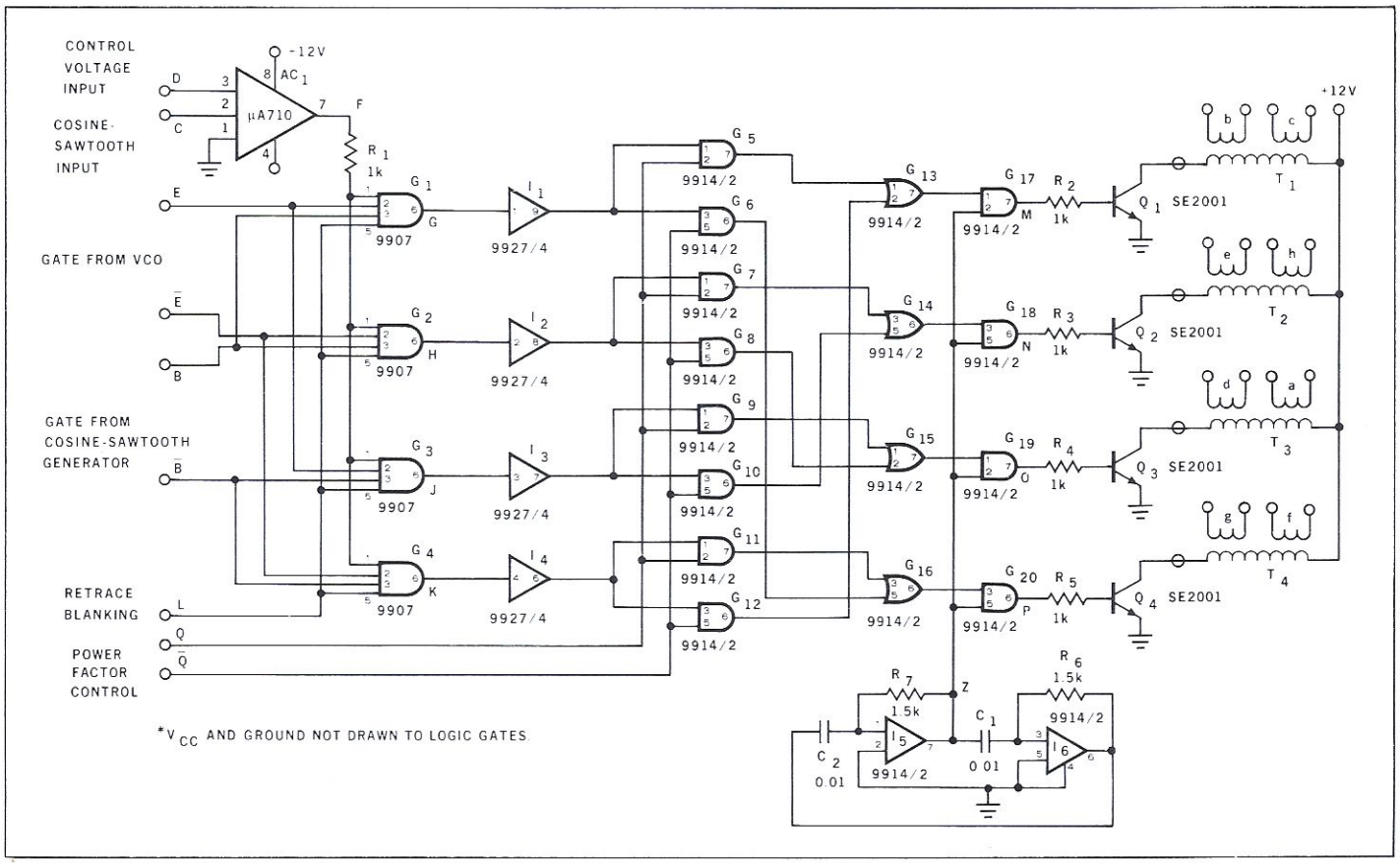

Fig. 7. Schematic of SCR gate signal comparator distribution gates, power factor control gates, modulator, and SCR gate drivers.

SCR DRIVING GATES

The composite SCR gate driving signal is formed in a comparator utilizing a μA710 (AC_1 shown in Fig. 7). The cosine-sawtooth voltage is introduced at pin 2 or the non-inverting input to the comparator, while the rectified sine wave control voltage is introduced on pin 3, the inverting input. This connection to the comparator results in an output that goes from a +3 volt level to a -0.7 volt level when the rectified sine wave control voltage is greater than the cosine-sawtooth voltage. This output voltage is then introduced into one input on each of the four quad input gates consisting of μL9907's (G_1, G_2, G_3, and G_4). Also introduced into appropriate inputs on the same gates are the complementary gating signals from the VCO (E). The zero crossing comparator (B) and the cosine-sawtooth retrace blanking signal (L). The four outputs from these gates are inverted in a μL9927 (I_1, I_2, I_3, I_4) and the resulting inverted signals are then supplied to the power factor control gates. These gates determine whether the positive or negative group SCR's will be turned on as necessitiated by the actual load demand. The complementary gating signals that provide proper control are generated in the power factor control circuitry. The power factor control circuitry is shown on Fig. 8. T_5 is a magnetic pickup transformer in which the primary consists of a single turn in one side of the power line. The voltage produced in the secondary is in-phase with the line current. This is amplified and compared with ground in AC_1 to produce $\overline{R}$. The inverter Q_1 produces the R term. R then will be true when the load current is negative. The signal R is then combined with a signal that indicates polarity of the load voltage (E) to produce the power factor control signals, $\overline{Q}$ and Q. $\overline{Q}$ will be false (or low) when there exists the special cases of load voltage positive and load current negative, or load voltage negative and load current positive. When the load is resistive, Q will normally be true (or low). Signals Q and $\overline{Q}$ are then used to switch the SCR gate firing signals to the proper SCR groups as dictated by load current. The power factor SCR gate switching is accomplished in logic gates G_5 through G_{16} (Fig. 7). These gates multiplex SCR gate signals G, H, J, and K and produce signals M, N, O, and P, depending upon the states of Q and $\overline{Q}$.

The four output signals from the power factor control gates are supplied to the carrier modulators. These four "AND" gates (G_{17}, G_{18}, G_{19} and G_{20}) combine the output from the power factor control gates and a 100-kc signal from a free-running multivibrator. The free-running multivibrator is composed of a single μL9914 (I5, I6) two resistors (R_6, R_7) and two capacitors (C_1, C_2). The gated 100-kc carrier is then used to drive the primaries of the SCR gate

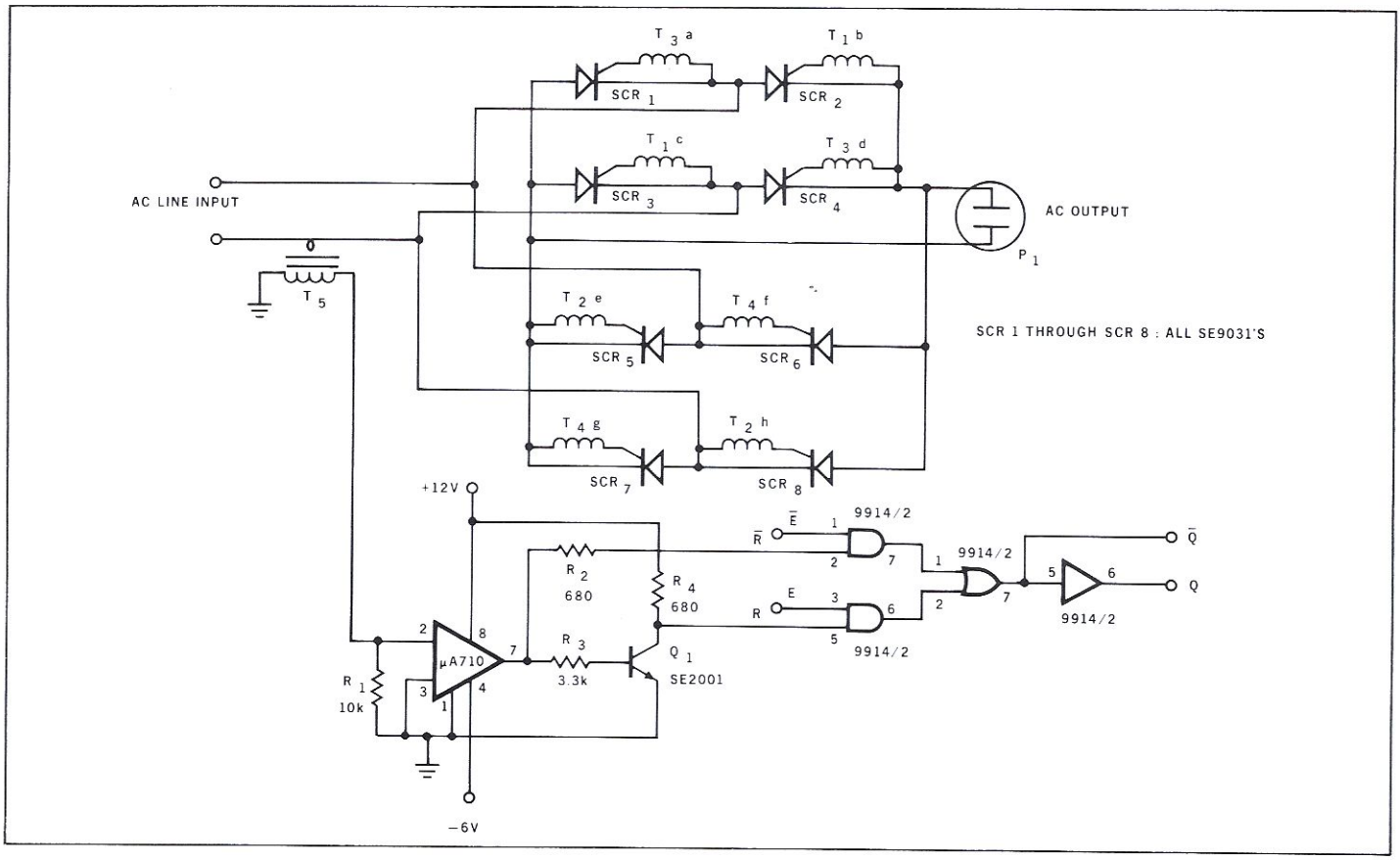

Fig. 8. Schematic diagram of SCR power control gates and power factor control generator.

transformers through the use of the discrete drive transistors, Q_1, Q_2, Q_3, and Q_4. The SCR gate transformers provide the essential gate signal coupling, and high-voltage isolation needed for proper operation of the SCR power gates.

SCR POWER GATES

Transformer T_1 is used to couple gate signals to SCR2 and SCR3 (Fig. 8). Transformer T_2 couples the gate signals to SCR5 and SCR8. Transformer T_3 drives the gates of SCR's 1 and 4. Transformer T_4 couples the gate signal to SCR's 6 and 7. The SCR's 1 through 8 form a full wave bridge capable of giving either polarity at the load regardless of the polarity of the input power line.

For a purely resistive load in which the current follows the voltage and the power factor signals Q and $\overline{Q}$ are true, the following statements will be correct. When the power line is instantaneously positive and it is desired to have the same polarity across the load, SCR2 and SCR3 will be fired. With the power line again positive but a reversal of polarity desired at the load, SCR5 and SCR8 will be fired. SCR's 6 and 7 will be fired if the power line is instantaneously negative and the same polarity is desired at the load. SCR's 1 and 4 will fire for a negative power line, but will produce polarity reversal at the load.